DIGITAL ELECTRONICS

II Year II Semester: IT/CSIT

Course Code	Category	Hours / Week			Credits	Maximum Marks		
		L	T	P	C	CIE	SEE	Total
A5EC71	ESC	4	0	0	4	30	70	100

COURSE OBJECTIVES:

The course should enable the students to:

1. Understand numerical and character representations in digital logic including ASCII and error detecting and correcting codes.
2. Design combinational and sequential logic circuits
3. Optimize combinational and sequential logic circuits.
4. Analyze a memory cell and apply for organizing larger memories

COURSE OUTCOMES:

1. Understand the different switching algebra theorems and apply them for logic functions.
2. Define the Karnaugh map for a few variables and perform an algorithmic reduction of logic functions.
3. Define the following combinational circuits: buses, encoders/decoders, (de)multiplexers, exclusive-ORs, comparators, arithmetic-logic units.
4. Understand the bistable element and the different latches and flip-flops.
5. Understand sequential circuits, like counters and shift registers.

UNIT-I NUMBER THEORY Classes: 12

Representation of numbers of different radix, conversion of numbers from one radix toanother radix, r-1‘s complement and r‘s complement of unsigned numbers subtraction, problem solving. problem solving for addition and subtraction. 4-bit codes: BCD, EXCESS 3, alphanumeric codes, 9‘s complement

UNIT-II BOOLEAN ALGEBRA LOGIC SIMPLIFICATION Classes: 14

Basic Theorems and Properties of Boolean algebra, Switching Functions, Canonical and Standard Forms, Algebraic Simplification of Digital Logic Gates, Properties of XOR Gates, Universal Logic Gates. Multilevel NAND/NOR realizations. K- Map Method, up to five variable K- Maps, Don’t Care Map Entries, Prime and Essential prime Implications.

UNIT-III COMBINATIONAL LOGIC CIRCUITS DESIGN Classes: 16

Design of Half adder, full adder, half subtractor, full subtractor, Design of decoder, demultiplexer, higher order demultiplexing, encoder, multiplexer, higher order multiplexing, realization of Boolean functions using decoders and multiplexers, priority encoder, 4-bit digital comparator.

UNIT-IV SEQUENTIAL LOGIC DESIGN-I Classes: 16

Difference between combinational and sequential circuits, Classification of sequential circuits (synchronous and asynchronous); basic flip-flops, truth tables and excitation tables (nand RS latch, nor RS latch, RS flip-flop, JK flip-flop, T flip-flop, D flip-flop with reset and clear terminals). Conversion of flip-flops to other flip-flops.

UNIT-V SEQUENTIAL LOGIC DESIGN-II Classes: 16

Design of Ripple counters, design of synchronous counters, Johnson counter, ring counter, shift register,

bi-directional shift register, universal shift register. Ripple and Synchronous counters, Finite state machines, Design of synchronous FSM, Algorithmic State Machines charts. Designing synchronous circuits like Pulse train generator, Pseudo Random Binary Sequence generator, Clock generation.

TEXT BOOKS:

1. Switching and Finite Automata Theory- Zvi Kohavi & Niraj K. Jha, 3rd Edition, Cambridge.
2. Digital Design- Morris Mano, PHI, 3rd Edition.

REFERENCE BOOKS:

1. Introduction to Switching Theory and Logic Design – Fredriac J. Hill, Gerald R. Peterson, 3rd Ed,John Wiley & SonsInc.
2. Digital Fundamentals – A Systems Approach – Thomas L. Floyd, Pearson, 2013.
3. Digital Logic Design - Ye Brian and HoldsWorth, Elsevier 4. Fundamentals of Logic DesignCharles H. Roth, Cengage LEanring, 5th, Edition, 2004.